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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/877,792 | 06/08/2001 | Hector Sanchez | SC11391TC | 6921 |

23125 7590 06/02/2005

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| EXAMINER | |
|---|---|
| PROCTOR, JASON SCOTT | |
| **ART UNIT** | **PAPER NUMBER** |
| 2123 | |

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/877,792 | SANCHEZ ET AL. | |
| | Examiner | Art Unit | |
| | Jason Proctor | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *22 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *7 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050419* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-37 were submitted for examination and rejected in non-final office action dated October 21, 2004. In Applicants' response dated February 22, 2005, claims 1, 2, 36 and 37 have been amended. Claim 8 has been canceled. No claims have been added. In telephone interview on April 18, 2005, Applicant has clarified that claim 7 has been canceled as indicated by Applicants' Remarks, page 16. Claims 1-6 and 9-37 are currently pending. Claims 1-6 and 9-37 have been rejected.

### *Objection to the Drawings*

The Examiner thanks Applicant for amending the drawings in response to the previous objections. Those objections have been withdrawn.

### *Objection to the Specification - Informalities*

The Examiner thanks Applicant for amending the specification in response to the previous objections. Those objections have been withdrawn.

1. Regarding the objection related to equation 3 and the specification at page 8, lines 19-26, it appears as though the amendments to the specification introduce new informalities. Specifically, it appears that the amended equation 3 on page 7, lines 5-7

now includes the term "*K10 K*10•*C* int $^{c\ int\_tx}$ • *Tx*", which does not correspond to the specification at page 8, lines 19-26.

***Objection to the Specification – Antecedent Basis***

The Examiner thanks Applicant for clarification regarding the support for the claim terminology. The Examiner kindly thanks Applicant for the citations of 37 CFR 1.75(d)(1) and MPEP 608.01(o). As Applicant has correctly identified, the basis for these objections were found in numerous terms used to refer to "power supply voltage" and "metallization resistance and capacitance". Applicants' clarification has established the similar meanings of these numerous terms; therefore these objections have been withdrawn.

The Examiner thanks Applicant for amending the phrase "running experiments using the performance model" to the more precise "performing timing analyses". The related objection has been withdrawn.

The Examiner agrees that the objection to the phrase "transistor impedance" is moot in light of Applicants' amendment. That objection has been withdrawn.

***Claim Objections***

The Examiner thanks Applicant for amending the claims in response to the previous objections to claims 36 and 37. The objections to claims 36 and 37 have been withdrawn.

2. The apparent typographical error of claim 1 indicated by the previous objection to that claim is still found in amended claim 1. The objection to claim 1 has been maintained.

### *Claim Rejections – 35 U.S.C. § 101*

Based on Applicants' arguments, these rejections are withdrawn.

### *Claim Rejections – 35 U.S.C. § 112, First Paragraph - Enablement*

Regarding the rejections of claims 1, 36, and 37 as being based on a disclosure which is not enabling, Applicant argues that:

> As taught by Applicants in the specification, transistor performance fluctuates based upon the manufacturing process used to create the transistor as well as subtle variations in a particular manufacturing process. These fluctuations are well known to those skilled in the art. Applicants further note that in the background of Applicants' application (pages 1-2), Applicants describe the timing rule currently used in the art today evaluates an equation in the form of:
>
> Equation 1 $Delay = (K1 + K2 \bullet Cl) \bullet Tx + K3 \bullet Cl^2 + K4 \bullet Cl + K5$
>
> This prior art equation takes into account the process used to create the transistor. Therefore, it is clear that the "process" parameter is a well known parameter to those skilled in the art and, consequently, Applicants submit that Applicants' claimed invention is enabled to those of skill in the relevant art. (see 35 U.S.C. § 112, MPEP §§ 706.03 and 2164).

At issue was the meaning of the phrase "related to transistor performance", as effectively recited by exemplary claim 1, which the Examiner has apparently interpreted

too narrowly. It is clear from Applicants' arguments this terminology **does not mean** an equation wherein a variable is directly substituted for "transistor performance", but rather **does mean** an equation wherein a variable is *related*, as would be recognized by a person of ordinary skill in the art, to "transistor performance". The Examiner apologizes for the unduly narrow interpretation of the phrase. The Examiner does not challenge that Applicants' disclosure is enabled for the phrase as argued by Applicant.

Based on Applicants' arguments, these rejections are withdrawn.

Regarding the recited steps of "making an integrated circuit", the Examiner thanks Applicant for clarification that the circuit is made by processes old and known in the art. The Examiner does not challenge that Applicants' disclosure is enabled for that interpretation.

The Examiner thanks Applicant for clarification regarding the interpretation of the claim language. The previous rejections under 35 U.S.C. § 112, first paragraph, for enablement have been withdrawn.

***Claim Rejections – 35 U.S.C. § 112, First Paragraph – Best Mode***

Regarding the rejection of claims 1-37 as failing to disclose the best mode contemplated by the inventor, Applicant remarks on page 19:

> As an initial matter, Applicants are highly offended that the Examiner rejected Applicants' claims as failing to disclose the best of Applicants' invention.

Applicant remarks on page 20:

> Instead, the Examiner points to certain characteristics of Applicants' equations and contends that, for some convoluted reasons, the equations show that the Applicants' failed to disclose the best mode of practicing the invention.

Applicant further remarks on page 20:

> As previously stated, Applicants are highly offended at the Examiner's contention that Applicants failed to disclose the best mode, as known by the Applicants, for practicing Applicants invention. Applicants respectfully insist that the Examiner immediately withdraw this offensive and completely unfounded rejection.

The Examiner meant no personal offense whatsoever in making these rejections in the previous office action. The Examiner apologizes for any perceived offense.

Based on Applicants' arguments, these rejections are withdrawn.

***Claim Rejections – 35 U.S.C. § 112, Second Paragraph - Indefiniteness***

Regarding the rejection of claims 1-37 under 35 U.S.C. § 112, second paragraph, as being vague and/or indefinite, the Examiner thanks Applicant for clarification of the claim language. The Examiner thanks Applicant for citing support in the specification for the limitations in question. Referring to claim 1 as exemplary of 37, the limitation under discussion is (emphasis added):

> Applying the circuit simulator to the first circuit design to derive a first set of constants for the plurality of constants

This limitation is represented in claim 36 as:

> Means for determining values for one or more of the unknown constants, the determined values being a first set of constants

It is clear from Applicants' arguments and the disclosure of the invention that this terminology **does not mean** an a circuit simulator that derives a first set of constants for the plurality of constants but rather **does mean** steps wherein a human operator makes

use of the circuit simulator to derive the first set of constants for the plurality of constants. Support for this is found as cited by Applicant (page 19, line 3) as well as at page 20, lines 11-25. Although the Examiner would prefer claim language that is not open to an interpretation wherein the circuit simulator derives constants, the Examiner thanks Applicant for this clarification and withdraws the previous rejections under 35 U.S.C. § 112, second paragraph.

***Remarks Regarding Rejections under 35 U.S.C. §§ 102 and 103***

In addition to responding to Applicants' arguments regarding the rejections under 35 U.S.C. §§ 102 and 103, traversed below, the Examiner respectfully observes that claim 1 does not recite the disclosed invention as necessary, critical, or relevant to the outcome of the method.

Claim 1 recites "a method for making an integrated circuit", comprising various steps, but concluding with the steps of "changing the first circuit design to obtain a second circuit design; and making an integrated circuit comprising the second circuit design". The intervening steps, which do recite Applicants' disclosed invention, have no positively recited contribution to the integrated circuit that results from the claimed method. Indeed, a person of ordinary skill in the art would recognize the step of "changing the first circuit design to obtain a second circuit design" as broad enough to cover nonfunctional "changes" to the circuit design, effectively reducing the contribution of Applicants' disclosed invention to nothing.

As a result, the limitations relating to Applicants' disclosed invention cannot be granted patentable weight as recited by claim 1. Claim 1 recites a method for making an integrated circuit comprising three critical steps: providing a first circuit design, changing the first circuit design to obtain a second circuit design, and making an integrated circuit comprising the second circuit design.

These remarks do not constitute new grounds of rejection. The Examiner maintains the traversals given below regarding the rejections of 35 U.S.C. §§ 102 and 103, but respectfully remarks that a limitation-by-limitation mapping of the prior art to claim 1 is beyond what is required to show anticipation or obviousness due to the form of the claim. The Examiner has applied prior art to the recited limitations and traversed Applicants' arguments regarding the same in the interests of compact prosecution. The Examiner respectfully suggests that Applicant review the form of the claim as regards the disclosed invention and the patent protection sought by Applicant.

### *Claim Rejections – 35 U.S.C. § 102*

Regarding the rejection of claims 1-3, 36, and 37 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,883,818 to Salimi et al. (Salimi), Applicant argues primarily that:

> Salimi clearly does not teach or suggest "changing the first circuit design to obtain a second circuit design" as claimed by Applicants. Instead, Salimi is focused on improving the modeling function that corresponds with a given logic cell (circuit). Nowhere does Salimi teach or suggest creating a second logic cell (circuit) based on any of the steps performed by Salimi. Indeed, the stated purpose of the Salimi patent is "to improve the accuracy of the ... equation" (col. 1, lines 38-43).

3. The Examiner respectfully traverses Applicants' arguments as follows:

The following is a quotation of MPEP 2112:

> The express, implicit, and inherent disclosures of a prior art reference may be relied upon in the rejection of claims under 35 U.S.C. 102 or 103. "The inherent teaching of a prior art reference, a question of fact, arises both in the context of anticipation and obviousness." *In re Napier*, 55 F.3d 610, 613, 34 USPQ2d 1782, 1784 (Fed. Cir. 1995) (affirmed a 35 U.S.C. 103 rejection based in part on inherent disclosure in one of the references). See also *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ 769, 775 (Fed. Cir. 1983).

As would be recognized by a person of ordinary skill in the art, a method for generating a timing model for an integrated circuit (column 1, lines 47-48) is a step of designing an integrated circuit. It is explicitly recited that Salimi's invention is to be used in the process of designing an integrated circuit. See, for example, Salimi, column 1, lines 7-10. There is no useful art of generating a timing model for an integrated circuit for the sake of appreciating the model. A timing model is a tool used to design an integrated circuit.

Applicants' arguments on this point are unpersuasive.

Applicant further argues:

> In other words, Salimi teaches a method of creating a more accurate model that is used to model a circuit design. Important, however, is the fact that nowhere does Salimi teach or suggest creating a new or modified circuit, in sharp contrast to Applicants' claimed invention in both claims 1 and 37 [...]"

4. The Examiner respectfully traverses Applicants' arguments as follows:

Salimi, column 1, lines 7-10 recite (emphasis added) "The present invention relates, in general, to the <u>design of integrated circuits</u> and, more particularly, to methods for generating models for evaluating the operation of an integrated circuit design." Although Salimi may not explicitly recite the words "creating a new or modified circuit",

the act of designing an integrated circuit inherently involves creating a new or modified circuit when, after evaluating the operation of an integrated circuit design, it is found that the first design is unsatisfactory in some regard.

Applicants' arguments on this point are unpersuasive.

The rejections under 35 U.S.C. § 102 are maintained.

***Claim Rejections – 35 U.S.C. § 103***

Regarding the rejection of claims 1-12 under 35 U.S.C. § 103 as obvious over US Patent No. 6,090,152 to Hayes et al. (Hayes) in view of US Patent No. 6,161,211 to Southgate (Southgate), claims 13-24 as obvious over Hayes in view of Southgate in further view of US Patent No. 6,507,935 to Aingaran et al. (Aingaran), and claims 25-35 as obvious over Hayes in view of Southgate in further view of US Patent No. 5,559,715 to Misheloff (Misheloff), Applicant argues primarily that:

> Regarding claim 1, Hayes teaches a system and method for using logical "adders" to account for variations in operating conditions during timing simulations. Hayes specifically teaches away from using multiplicative derating factors to model voltage and temperature effects on timing performance. Throughout the Hayes reference, Hayes teaches away from using multiplicative derating factors to model performance. In the "Abstract," Hayes unequivocally teaches that "***Rather than using***, the prior art approach of ***multiplicative derating factors to model voltage and temperature effects on timing performance***, adders are used to model the change in performance due to variations in operating conditions (i.e., voltage and temperature)." (emphasis added). In sharp contrast, Applicants claim provides an equation that comprises a number of variables that include multiplicative constants related to voltage and temperature.

5. The Examiner respectfully traverses Applicants' arguments as follows:

The Examiner disagrees with Applicants' argument that the claim provides an equation that comprises a number of variables that include multiplicative constants related to voltage and temperature. The claim fails to provide any such equation. Regardless, the Examiner disagrees with Applicants' distinction between Applicants'

invention and the Hayes reference. Hayes discloses many equations that comprise "a number of variables that include multiplicative constants related to voltage and temperature" (Equation 4, column 5, line 35; Equation 5, column 5, line 53; Equation 6, column 5, lines 59-64; Equation 7, column 6, lines 4-8). Hayes discloses a DCL code section that "illustrates the method used to calculate propagation delay and output transition time" which clearly shows a number of "multiplicative constants related to voltage and temperature" (column 8, lines 7-29). Applicants' arguments on this point are unpersuasive.

Applicant further argues:

> In short, Hayes does teach calculating a delay through a circuit, but does so in a manner completely different from that taught and claimed by Applicants. Namely, Hayes does not teach "providing an equation which comprises a plurality of variables and constants, wherein the plurality of constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature," as taught and claimed by Applicants.

6. The Examiner respectfully traverses Applicants' arguments as follows:

The Examiner appreciates Applicants' acknowledgement that Hayes teaches calculating delay through a circuit, however the independent claims of the instant application are not limited to and do not explicitly recite the method taught by the disclosure. Regarding the equation which comprises a plurality of variables and constants, Applicants' attention is respectfully drawn to Hayes, column 5, line 66 – column 6, line 9 and column 6, line 64 – column 7, line 12 as cited in the original rejection under 35 U.S.C. § 103(a) as unpatentable over Hayes in view of Southgate.

These citations teach the limitation quoted by Applicant. Applicants' arguments on this point are unpersuasive.

Applicant further argues:

> The Office Action admits that Hayes does not teach changing the design of the circuit, nor does Hayes teach making the circuit. Instead, the Office Action contends that Southgate teaches these limitations. Applicants disagree.
>
> and
>
> Southgate teaches writing the "blocks" in a file format such as VHDL or Verilog (col. 6, lines 16-21). While these Verilog or VHDL blocks describe the behavior of a block, they do not provide or generate ***timing*** information. Southgate discusses this shortcoming of the blocks and discusses that further techniques are needed to gather and analyze timing data ***after*** the design blocks have been completely (positively) simulated (col. 6, line 55 – col. 7, line 9).

7. The Examiner respectfully traverses Applicants' arguments as follows:

Applicant is respectfully reminded that in traversing the rejection of claims 1, 36, and 37 under 35 U.S.C. § 112, first paragraph, as being based on a disclosure which is not enabling, Applicant has argued that the circuit is made by processes old and known in the art.

The Examiner has not included the Southgate reference to establish what is known in the art as an "iterative design process", that is, a design process where a proposed product is tested and if found unacceptable, redesigned. This design process iterates the design and testing steps until an acceptable design is produced, which is then manufactured. Southgate clearly teaches an iterative design process as cited by the Examiner. Applicants' claims recite, in effect, an iterative design process focused on the circuit design and a timing analysis. The Examiner maintains that such an iterative design process would have been obvious over the teachings of Southgate.

The Examiner has provided several references cited on PTO-892 that help to clarify the issue of "iterative design". These references are provided for Applicants' consideration but do not constitute new grounds of rejection.

The details of Southgate's implementation, such as the use of Verilog or VHDL, are not and were not relied upon by the Examiner in the determination that Southgate renders the claim limitation obvious.

Applicants' arguments on this point are unpersuasive.

Applicant further argues:

> In combining the references, the Examiner fails to explain how timing data generated by Hayes can be used in the VHDL/Verilog code blocks taught by Southgate.

8. The Examiner respectfully traverses Applicants' arguments as follows:

Applicant is correct that the Examiner has not explained the specific combination described by Applicant. However, this is not the teaching relied upon by the Examiner. As described above, Southgate teaches what is known in the art as an iterative design process. Applicants' arguments on this point are unpersuasive.

Applicant further argues:

> Applicants aver that the combination of Hayes and Southgate is improper in that it arose from the use of impermissible hindsight.

9. The Examiner respectfully traverses Applicants' arguments as follows:

The teaching of Southgate relied upon by the Examiner is that of an iterative design process, which is well known in the art. The Examiner asserts that it is not

impermissible hindsight to use well-known techniques that possess well-known advantages.

Applicant further argues that claims 13-24 and 25-35, depending from claim 1, are allowable based on the arguments for claim 1. The Examiner has respectfully traversed Applicants' arguments of claim 1 and therefore this argument is unpersuasive.

The rejections under 35 U.S.C. § 103 are maintained.

## *Outstanding Objections and Rejections*

### *Specification*

10. The abstract of the disclosure is objected to because equation 3 and the specification at page 8, lines 19-26, as amended, appear to conflict. Specifically, it appears that the amended equation 3 on page 7, lines 5-7 now includes the term "*K10* $K10 \bullet C \text{ int}^{c \text{ int\_}tx} \bullet Tx$", which does not correspond to the specification at page 8, lines 19-26.

Correction is required. Please see MPEP § 608.01(b).

### *Claim Objections*

11. Claim 1 is objected to because of the following informalities: The phrase "wherein the plurality constants are unknown constants" in claim 1, line 9 appears to contain a typographical error. The Examiner presumes this phrase should read

"wherein the plurality **of** constants are unknown constants", similar to amended claims 36 and 37. Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-3, 36, and 37 are rejected under 35 U.S.C. § 102(b) as being anticipated by Salimi et al., US Patent No. 5,883,818.

Regarding claim 1, Salimi et al. teaches a method for making an integrated circuit (column 3, lines 32-33) comprising:

providing a circuit simulator having the capability to of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 3, lines 39-44; Fig. 3, reference 200);

providing a first circuit design (column 3, lines 32-38);

providing an equation which comprises a plurality of variables and coefficients (column 3, lines 44-46; column 4, lines 22-46), wherein the plurality of coefficients are unknown coefficients (column 4, lines 47-51), and one of the variables is related to at least one of power supply voltage, distributed

capacitance, distributed resistance, transistor performance, and temperature (column 4, lines 22-46);

applying the circuit simulator to the first circuit design to derive a first set of coefficients for the plurality of coefficients (column 3, lines 46-49; column 4, lines 47-51; column 5, lines 33-38; Fig. 3, reference 210);

replacing the unknown coefficients with the first set of coefficients to obtain a performance model of the first circuit design (column 3, lines 46-47; column 5, lines 33-38; Fig. 3, references 210, 220);

performing a first set of timing analyses using the performance model of the first circuit design (column 3, lines 47-49; Fig. 3, references 220, 230);

changing the first circuit design to obtain a second circuit design (column 3, 59-64; column 5, lines 33-38; Fig. 3, references 220, 230, 240, 270, 290);

making an integrated circuit comprising the second circuit design (column 5, lines 45-49; column 3, lines 32-38; column 4, lines 18-19).

Examiner considers that evaluating the performance of at least a portion of one of the logic cells at different operating parameters to generate simulation data (column 1, lines 56-58) is equivalent to providing and applying a simulator.

Regarding claim 2, Salami et al. teaches:

applying the circuit simulator to the second circuit design to derive a second set of coefficients for the plurality of coefficients (column 3, line 59 – column 4, line 1; column 5, lines 32-38; Fig. 3, references 220, 230, 240, 270, 290);

replacing the first set of coefficients with the second set of coefficients to obtain a performance model of the second circuit design (column 3, line 59 – column 4, line 1; column 5, lines 32-38; Fig. 3, references 220, 230, 240, 270, 290); and

performing a second set of timing analyses using the performance model of the second circuit design (column 3, line 59 – column 4, line 20; column 5, lines 32-38, Fig. 3, references 220, 230, 240, 270, 290).

Regarding claim 3, Salami et al. teaches that the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature (column 4, lines 22-46).

Claim 36 is directed toward a computer readable medium and recites limitations generally corresponding to the method of claim 1. As Salimi et al. teaches a system for designing an integrated circuit embodied on a computer (Fig. 1; column 2, line 58 – column 3, line 6), claim 36 is rejected for reasons similar to those given for claim 1 above.

Claim 37 is directed toward a method for obtaining a performance model and recites limitations generally corresponding to the limitations of claims 1 and 2. As Salimi et al. teaches a method for obtaining a performance model (column 3, lines 46-47;

column 5, lines 33-38; Fig. 3, references 210, 220), claim 37 is rejected for reasons similar to those given for claims 1 and 2 above.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. US Patent No. 6,090,152 and further in view of Southgate US Patent No. 6,161,211.

Regarding claim 1, Hayes et al. teaches a method for predicting the performance of an integrated circuit design comprising:

providing a circuit simulator (column 6, lines 56-57) having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 6, lines 57-63);

providing a first circuit design (column 6, lines 45-53);

providing an equation which comprises a plurality of variables and coefficients (column 5, line 66 – column 6, lines 9);

wherein the plurality of coefficients are unknown coefficients (column 6, line 64 – column 7, line 12);

one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature (column 5, line 66 – column 6, line 9);

applying the circuit simulator to the first circuit design to derive a first set of coefficients for the plurality of coefficients (column 6, line 64 – column 7, line 12); and

replacing the unknown coefficients with the first set of coefficients to obtain a performance model of the first circuit design and performing timing analyses using the performance model of the first circuit design (column 7, lines 13-28).

Hayes et al. does not teach changing the design of the circuit or making the circuit.

Southgate teaches a method for designing a circuit represented by blocks (column 5, line 66 – column 6, line 4; column 6, lines 30-38) wherein a performance analysis is conducted, and if goals for the design have not been met, changing the first circuit design to obtain a second circuit design and making an integrated circuit comprising the second circuit design (column 6, line 55 – column 7, line 9; Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to incorporate the redesign and manufacture steps of Southgate's invention into the circuit simulation and performance modeling method of Hayes et al. in

order to produce a method that makes effective and efficient use of the results provided by the invention of Hayes et al. The combination could readily be achieved by making adjustments to the circuit design based on the modeling results and making the resulting integrated circuit by methods known in the art.

Regarding claim 2, Hayes et al. does not teach applying a circuit simulator to the second circuit design to derive a second set of coefficients, replacing the first set of coefficients with a second set of coefficients, and running experiments using the performance model of the second circuit design. However, the combination formed in the rejection of claim 1 anticipates this method. Having made adjustments to the circuit design based on the modeling results, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to subject the second circuit design to the same process as the first circuit design, and if it meets the performance goals, make a circuit according to the second design.

Performing this process with the invention of Hayes et al. would comprise:

applying the circuit simulator to the second circuit design to derive a second set of coefficients for the plurality of coefficients;

replacing the first set of coefficients with the second set of coefficients to obtain a performance model of the second circuit design; and

performing timing analyses using the performance model of the second circuit design.

Regarding claim 3, Hayes et al. teaches that the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature (column 5, line 66 – column 6, line 9; column 6, line 64 – column 7, line 12; column 7, lines 13-16; column 7, lines 37-41).

Regarding claims 4-6 and 9-12, Hayes et al. teaches that the equation comprises a plurality of delay expressions (column 5, line 35, equation 4; column 5, line 52, equation 5; column 5, lines 60-63, equation 6; column 6, lines 5-7, equation 7).

2. Claims 13-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. in view of Southgate as applied to claim 1 above, and further in view of Aingaran et al. US Patent No. 6,507,935.

Regarding claims 13-24, neither Hayes et al. nor Southgate explicitly teach a plurality of capacitance expressions.

Aingaran et al. teaches a plurality of capacitance expressions (column 5, line 25 – column 6, line 60; column 11, lines 1-19). It would have been obvious for a person of ordinary skill in the art at the time of applicant's invention to combine the modeling equations of Aingaran et al. with the combined invention of Hayes et al. and Southgate in order to better simulate the performance of the circuit being designed.

3. Claims 25-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayes et al. in view of Southgate as applied to claim 1 above, and further in view of Misheloff, US Patent No. 5,559,715.

Regarding claims 25-35, neither Hayes et al. nor Southgate explicitly teach a plurality of setup/hold time expressions.

Misheloff teaches setup/hold time expressions (column 16, line 58 – column 17, line 21). It would have been obvious for a person of ordinary skill in the art at the time of applicant's invention to combine the modeling equations of Misheloff with the combined invention of Hayes et al. and Southgate in order to better simulate the performance of the circuit being designed.

***Conclusion***

Art considered pertinent by the examiner but not applied has been cited on form PTO-892. The Examiner has changed the language of the rejections under 35 U.S.C. §§ 102 and 103 to only to accurately reflect Applicants' amended claim language, accordingly **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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